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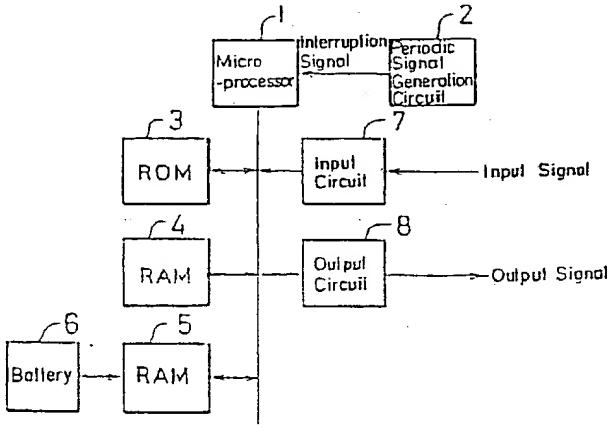
(71) Applicant: **FANUC LTD, 3580, Shibokusa Aza-Komanba Oshino-mura, Minamitsuru-gun Yamanashi 401-05 (JP)**

(72) Inventor: **INOUE, Michiya, 5-28-6, Hirayama Hino-shi, Tokyo 191 (JP)**
Inventor: **YAMAUCHI, Takashi Fanuc Manshion Harimomi 6-202, 3537-1, Shibokusa Oshino-mura, Minamitsuru-gun Yamanashi 401-05 (JP)**

(74) Representative: **Brunner, Michael John et al, GILL JENNINGS & EVERY 53-64 Chancery Lane, London WC2A 1HN (GB)**

(54) PLC APPARATUS.

(57) A PLC apparatus for executing sequence programs using a microprocessor (1). The PLC apparatus comprises a periodic signal generating circuit (2) for generating interrupt signals at regular intervals, an input circuit (7) for receiving input signals sent from an external unit, and filtering means for reading and filtering the signals from the input cirquit at regular intervals in response to the interrupt signals. The time constant of the filter for filtering based on the microprocessor is programmable and can be changed for every signal.



EP 0 321 575 A1

D E S C R I P T I O N

PLC DEVICE

Technical Field

The present invention relates to a PLC device for effecting arithmetic operations of a sequential program, and more specifically to a PLC device for processing a filtering of an input signal by a microprocessor.

Background Art

An input circuit of a PLC device is provided with a filter for removing noise and preventing malfunctions due to chatter or the like. The input circuit is provided with hardware filters. For example, a circuit arrangement comprising a low pass filter of an integration circuit composed of a resistor is generally used and a capacitor and an output thereof is shaped by a Schmitt circuit.

Nevertheless, since a filtering function effected by the conventional hardware filters requires a hardware filter circuit for each signal, the number of parts is increased, the cost of mounting becomes higher, and a larger space must be provided for mounting these parts. Further, the respective circuit elements must be changed to change a time constant of a filter, which is

practically impossible after the device has been assembled. This is inconvenient when the PLC devices are installed in various locations whereat a high level of noise occurs. In addition, a filter having a large time constant must be provided when an input signal has a low speed and a filter having a small time constant must be provided when an input signal has a high speed, but the need to mount filters having a different time constant for each signal on the same printed circuit board or the like complicates the manufacture of a filter hardware.

Disclosure of the Invention

An object of the present invention is to solve the above problems and to provide a PLC device for processing a filtering of an input signal by a microprocessor without using hardware filter.

To achieve the above object, in accordance with the present invention, there is provided as shown in FIG. 1, a PLC device for effecting arithmetic operations of a sequence program by a microprocessor (1): comprising a periodic signal generating circuit (2) for generating an interruption signal at a predetermined time interval; an input circuit (7) for receiving the external input signal; and filtering processing means for effecting a filtering process to a signal read from the input circuit at a predetermined time interval in response to the

interruption signal.

The microprocessor reads a signal from an input circuit at a predetermined time interval, processes a filtering of the signal and then takes in the as a signal to be processed. Accordingly, the hardware filter can be omitted and since the filtering processing is effected by the microprocessor, a time constant of a filter can be changed by a program, and can be also changed each time a signal is read.

Brief Description of the Drawings

FIG. 1 is a block diagram of an embodiment of the present invention;

FIG. 2 is a flowchart of an embodiment of the present invention; and

FIG. 3 is a time chart of a filtering process.

Best Mode for Carrying Out the Invention

An embodiment of the present invention will be hereinafter described in detail with reference to the drawings.

FIG. 1 is a block diagram of an embodiment of the present invention, wherein 1 designates a microprocessor effecting an overall control of a PLC device, and 2 designates a periodic signal generating circuit for generating an interruption signal at a

predetermined time interval. The microprocessor 1 processes a filtering of an input signal in response to the interruption signal and takes in the signal. Designated at 3 is a ROM for storing a system program, and the microprocessor 1 controls the PLC device in accordance with the system program of the ROM 3. 4 designates a RAM for a workpiece which stores various data or the like, and 5 designates a RAM for storing a sequential processing program. The sequential program is used for regulating a machine operation actually controlled by the PLC device, and can be changed in accordance with a change in the machine operation. The RAM 5 is also connected to a battery 6 to maintain the sequential processing program even if the power supply is accidentally turned off. Denoted at 7 is an input circuit having receiver circuits for receiving external input signals from the machine or the like and causing the microprocessor to read out the input signals through a bus. The respective receiver circuits of the input circuit 7 have either no filtering function or a filtering function having a small time constant, because the filtering process is effected by the microprocessor through software, as described later. Designated at 8 is an output circuit outputting signals for operating the machine or the like. With the PLC device as described above, the filtering function of the input circuit 7 is

not effected by hardware. Namely, the microprocessor 1 processes the filtering by taking in a signal from the input circuit 7 in response to an interruption signal from the periodic signal generating circuit 2, and as a result, a time constant or the like of the filter can be changed by merely changing the system program of the ROM 3. Further, the time constants of the filter can be easily changed because they are stored in the sequential program stored in the RAM 5, in a form of a parameter or the like.

Next, the operation of the microprocessor 1 will be described with reference to FIG. 2 which is a flowchart of the embodiment. As shown in the drawing, the microprocessor 1 sequentially and periodically effects the processes S1, S2 and S3 as described below.

(S1) takes in an input signal. Note, the input signal has been filtered.

(S2) effects arithmetic operations of the sequence program: Here it effects a sequential program for controlling the machine.

(S3) produces an output signal as a result of the sequential processing of the program and which signal controls the actual operation of the machine.

The processing flow then goes to the process S4 in response to an interruption signal from the periodic signal generating circuit 2 while the program for the

process S2 is effected.

Next, an example of a filtering process will be described with reference to Fig. 3, which is a time chart for the filtering process. In the drawing, the interruption signal is a signal output by the periodic signal generating circuit 2 to the microprocessor 1 in FIG. 1; the input signal is a signal read from the input circuit 7 by the microprocessor 1 in FIG. 1; and the taken-in signal is a signal used by the microprocessor 1 as an internal signal after being filtered by the microprocessor 1.

In the filtering process, when an input signal remains in the same state after two interruption signals have been produced (interruption signals for two clocks), the input signal is processed as a taken-in signal. For example, when the input signal at position A is high for only one clock, the taken-in signal is not changed but when the input signal at position B is high for two clocks, the taken-in signal is made to high. On the contrary, although the input signal at a position C is made low, the taken-in signal is not changed but remains high because the input signal is low for only one clock. When the input signal at position D is made high for two clocks, then the taken-in signal is made low. As described above, the filtering process prevents the appearance of the taken-in signal at the positions A and

C of the input signal. Further, the number of clocks for which the input signal can be ignored as the taken-in signal can be changed by the system program, and can be also changed in accordance with the property of the respective signals. Furthermore, the number of clocks can be stored in the sequential program as a parameter and changed later.

According to the present invention, as described above, since the input circuit is not provided with hardware filter circuits and the filtering process is effected by the microprocessor through software, no hardware parts are required. In addition, a time constant of the filter can be easily changed by the system program or the like with ease.

CLAIMS

1. A PLC device for effecting arithmetic operations of a sequential program by a microprocessor, comprising:

a periodic signal generating circuit for generating an interruption signal at a predetermined time interval;

an input circuit for receiving an external input signal; and

a filtering processing means for effecting a filtering process to a signal read from the input circuit at a predetermined time interval in response to the interruption signal.

2. A PLC device according to claim 1, wherein said filtering process changes an output of a taken-in signal when the input signal is changed for a prescribed time interval or more.

3. A PLC device according to claim 1, wherein said input circuit does not include a filtering function effected by hardware.

4. A PLC device according to claim 1, wherein said input circuit is provided with a filtering function having a small time constant.

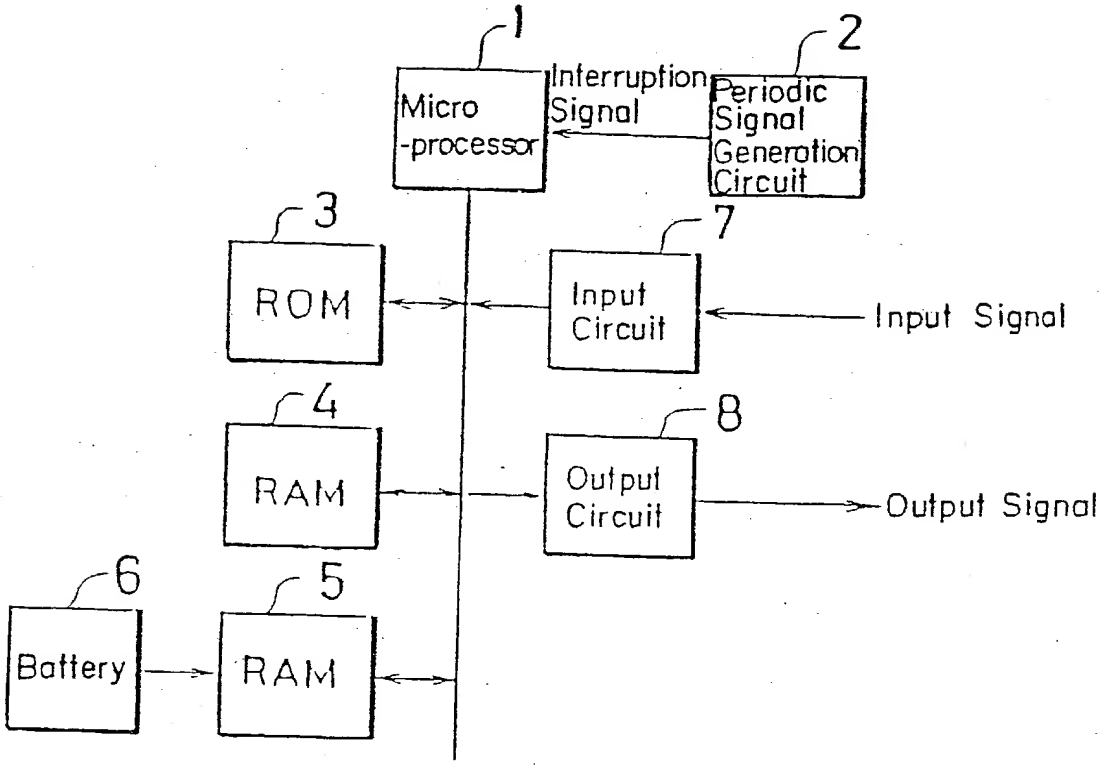

1
Micro
-processor
Interruption
Signal
2
Periodic
Signal
Generation
Circuit
3
ROM
7
Input
Circuit
Input Signal
4
RAM
8
Output
Circuit
Output Signal
6
Battery
5
RAM

FIG. 1

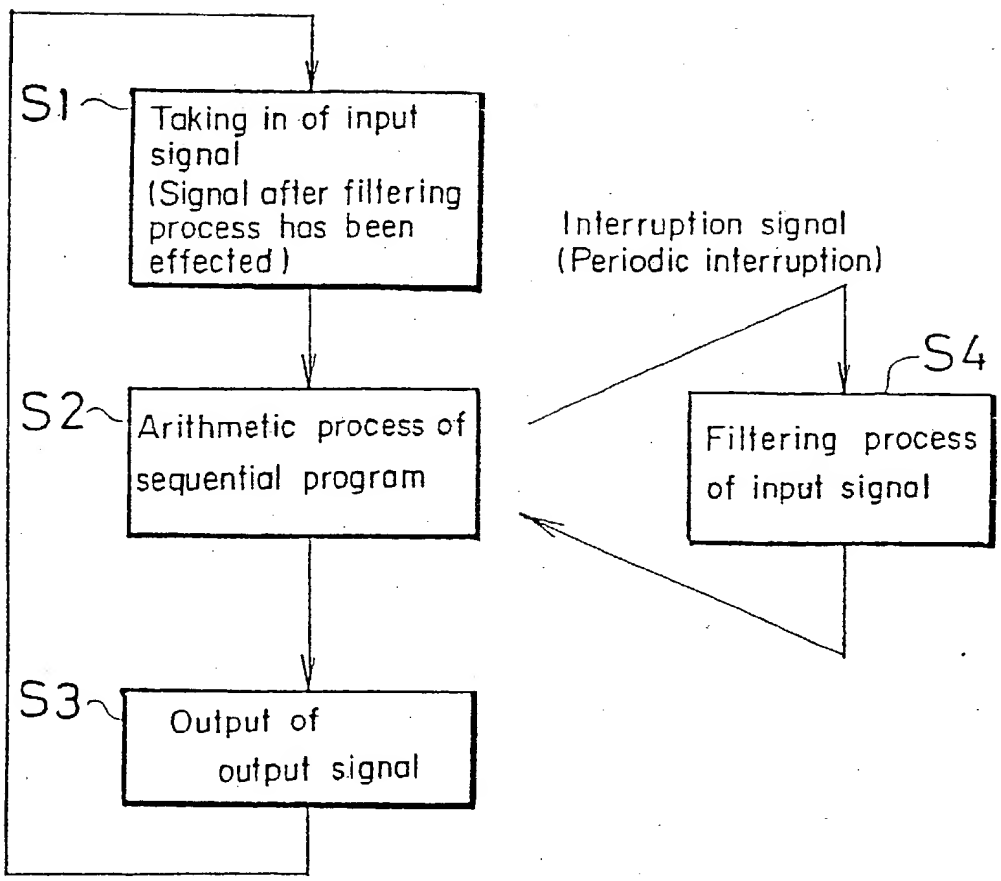

S1
Taking in of input signal (Signal after filtering process has been effected)
S2
Arithmetic process of sequential program
S3
Output of output signal
Interruption signal (Periodic interruption)
S4
Filtering process of input signal

FIG. 2

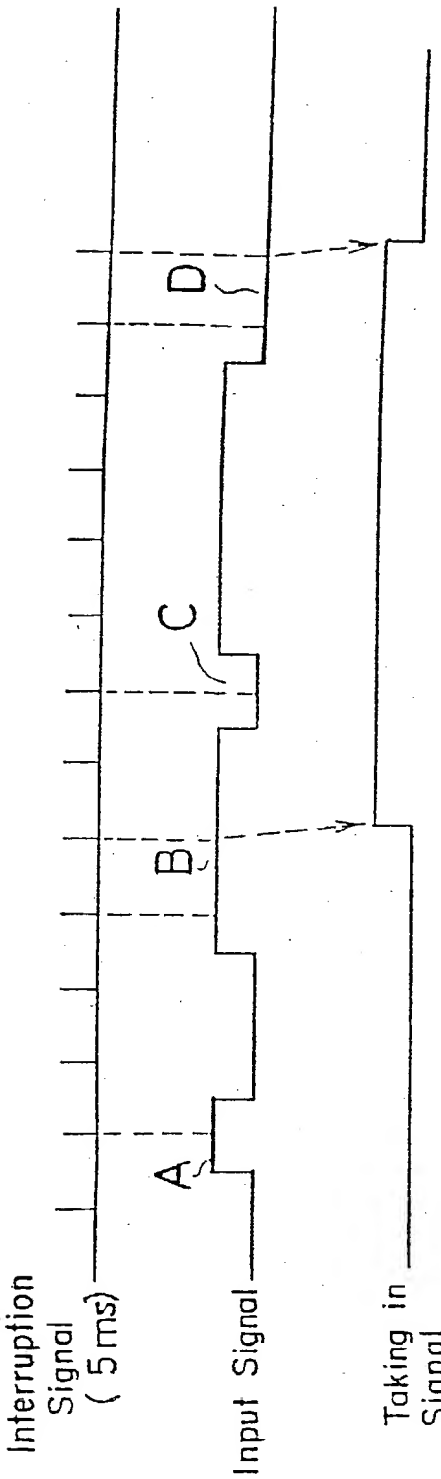

Interruption Signal (5ms)
Input Signal
Taking in Signal
A
B
C
D

FIG. 3

INTERNATIONAL SEARCH REPORT

International Application No PCT/JP88/00561

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl[4] G05B19/04

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC	G05B19/04

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

Jitsuyo Shinan Koho	1932 - 1988
Kokai Jitsuyo Shinan Koho	1971 - 1988

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	JP, A, 61-11802 (Fuji Electric Co., Ltd., Fuji Facom Seigyo Kabushiki Kaisha) 6 June 1986 (06. 06. 86) (Family: none)	1-4

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
September 2, 1988 (02. 09. 88)	September 19, 1988 (19. 09. 88)
International Searching Authority	**Signature of Authorized Officer**
Japanese Patent Office	